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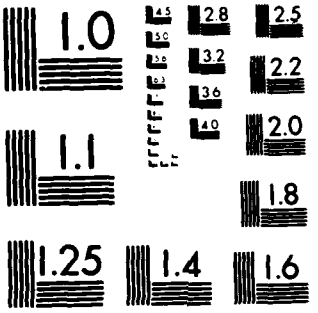

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Final Technical Report
February 1984

INVESTIGATION OF CHARGE COUPLED DEVICES FOR SIGNAL PROCESSING

University of Illinois

C. T. Sah

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ROME AIR DEVELOPMENT CENTER
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

New constant capacitance voltage transient methods are developed. Traps from ion implantation damage are profiled and characterized. New methods of determination of both majority and minority carrier capture rates at traps in one diode is developed. Two-dimensional numerical analyses with new boundary equations are demonstrated for micron and submicron silicon MOS devices. Dangling bound and hydrogen bonding of interface states and bulk dopant acceptor (boron) traps are experimentally demonstrated.

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I. INTRODUCTION

The objective of this basic reseach program is to delineate and project the performance capabilities of silicon CCD's for operation over wide temperature range, at increased speed, over large dynamic range and at higher chip functional density. The approach is to focus on experimental and theoretical characterization of the main material parameters which control the performance capabilities, such as trapping at shallow-level dopant impurities at low temperatures, trapping at interface, surface and bulk bound states, interband impact ionization effects in small geometry charge coupled devices, and others.

The contract included the following for a three-year study with an intention for a follow-up extension. However, due to budgetary problems, its starting date was delayed for nearly one year and due to redirection of contractor's programs, the intended extension was abandonded. Within these limitations, the following objectives have been attained.

(a) Develop experimental techniques (current transient, others) to characterize low temperature carrier trapping at shallow and deep levels which are relevant to the low temperature CCD operation.

(b) Use capacitance transient and other techniques to characterize the bulk traps commonly found in buried channel CCD (BCCD), and study effects of processing on the concentration of these traps, such as ion implantation, annealing and gettering.

(c) Measure the low field interband impact ionization rate on small geometry (2 micron channel or less) surface channel CCD's (SCCD) using a three-phase carousel geometry.

(d) Develop two-dimensional computer models which can lead to the prediction of the performance of SCCD and BCCD.

(e) Investigate the trapping at the interface states which could limit the performance of SCCD as well as BCCD.

Most of the research results have been published either as journal articles, or Air Force technical reports and doctoral theses. The latter can be obtained from the NTIS (National Technical Information Service) and University Microfilm, Inc. Ann Arbor, Michigan, respectively.

A summary of the research results are given in this final report. Chapter II describes the effort of developing constant capacitance voltage transient (CCVT) method to characterize multiple and closely-spaced levels. Chapter III describes the investigation of traps due to ion implantation damage using the CCVT method. Chapter IV summarizes the development of a new variation of the capacitance technqiue which permits very accurate determination of both majority and minority carrier capture and emission rates at a given level in only one diode which may contain multiple trapping levels. Chapter V gives a brief abstract of the effort on the characterization of low field impact ionization effect on CCD which was more fully reported in an AF technical report. Chapter VI summarized our efforts on the two-dimensional CAA (Computer-Aided-Analysis) modeling of micron and submicron MOS-type devices. Chapter VII reports the findings on interface states in oxidized silicon.

II. CONSTANT CAPACITANCE VOLTAGE TRANSIENT METHOD

Although the constant voltage capacitance transient (CVCT) method for trap characterization [1,2] is considerably simpler to implement in the laboratory compared with the constant capacitance voltage transient (CCVT) method, the capacitance transient method (CVCT) has a drawback which has been ignored by most experimenters who are only interested in a very qualitative detection of the trapping levels in a semiconductor or a semiconductor device. When an accurate determination of the trapping parameters, such as the thermal capture and emission rates, is needed, the capacitance transient method (CVCT) becomes inadequate since the decay of the capacitance could be highly non-exponential, making it difficult to determine accurately the real capture and emission rates at the traps. Several factors are responsible for an experimental non-exponential decay. (i) The concentration of the trap is high and comparable with the concentration of the majority dopant impurity. (ii) The concentration of the trap is high but also varies rapidly with position such as the case of traps due to ion implantation damage which have highly peaked trap concentration profiles. (iii) There are many trapping levels and their energy level spacings are not large compared with kT. (iv) The thermal capture and emission rates are highly dependent on electric field which gives rise to nonlinear or nonexponential decays since the electric field is highly position dependent in the depletion layer of a semiconductor junction space charge layer.

The constant capacitance voltage transient (CCVT) method overcomes some of these limitations, especially (i), (ii) and (iv). In view of these unique features of CCVT and the fact that multiple energy level traps are created by ion implantation in micron and submicron silicon VLSI-VHSIC devices and integrated circuits, including CCD's, an intensive effort was undertaken in this contract to develop the CCVT method so that it can be used as a straight-forward measurement tool to characterize the deep and shallow defect and impurity levels. This effort was highly sucessful due to the help of two experienced visiting professors from China (Professor Ming-Fu Li of the Chinese Academy of Science and Professor Kuo-Gang Qin of the Physics Department of Peking University who is also the director of their Semiconductor Research Laboratory). Both the experimental procedure and computer-controlled instrumentation for the CCVT method are now routine in our laboratory (to be referred to as ISSEL = Illinois Solid State Electronics Laboratory). In addition, the theory and its range of validity are developed to interpret the experimental data in diodes which have multiple and closely spaced carrier-recombination-generation energy levels in the silicon energy gap.

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1. C. T. Sah, L. Forbes, L. L. Rosier and A. F. Tasch, "Thermal and optical emission and capture rates and cross sections of electrons and holes at imperfection centers in semiconductors from photo and dark junction current and capacitance experiments," Solid-State Electronics, Vol.13(6), 759-788, June 1970.
2. G. L. Miller, D. V. Lang and L. C. Kimerling, "Capacitance transient spectroscopy," Annual Review of Material Science, Vol.7, 377-447, 1977.

The new technique is fully described in two publications by Prof. Li [3,4] which included not only the theory and experimental verification, but also detailed circuit modifications required of the commercial Boonton 72A one-Mega Hertz capacitance meter. A brief summary is given below.

The new technqiue employs a capacitance feedback circuit controlled by a digital computer to keep the high-frequency (one MHz) capacitance of a test diode constant after the trapped charge density is changed by a voltage step, light, or other perturbation. The capacitance is kept constant by varying the d.c. applied voltage to the diode. This voltage transient is sampled by a high-precision and high-speed digital voltmeter controlled by a Hewlett Packard 1000 minicomputer. The data are stored in a file and later analyzed by a nonlinear least-squares fit routine.

The principle reason for the advantage of the CCVT method is that when the high-frequency capacitance of the diode is kept constant during and after a perturbation is applied, the space charge layer thickness and the electric field distribution in the p/n junction of the diode are both constant. As a consequence, the voltage transient (required to keep the capacitance constant) is truly equal to or proportional to the decay of the trapped charge density at the defect or impurity levels in the space charge layer of the junction. There are no higher order dependences of the voltage transient on the trapped charge transient.

An extension of the data analysis of the voltage transient is made so that it can yield accurate depth profiles of the trap concentration. In order to do this, the contribution of the trapped charges in the edge region of the space charge layer must be accounted for since it affects the magnitude of the voltage decay whose time dependence come from trapping or detrapping at the traps in the depletion layer of the space charge layer. A theoretical method of correcting for the contribution from this nearly equilibrium edge region was developed and demonstrated by Sah and Neugroschel in 1975 [5]. This was simple to use but an experimental method would be more desirable. There are several experimental methods. What is required is another set of Capacitance-Voltage data to the CCVT data. Professor Li developed one scheme using the quasi-static capacitance-voltage (QSCV) data [4] and Professor Qin developed another scheme using the multiple-frequency capcitance-voltage (MFCV) data [6]. Both work well and the QSCV was tested and reported [4].

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3. Ming-Fu Li and C. T. Sah, "New techniques of capacitance-voltage measurements of semiconductor junctions," Solid-State Electronics, Vol. 25(2), 95-99, February 1982.
4. Ming-Fu Li and C. T. Sah, "A new method for the determination of dopant and trap concentration profiles in semiconductors," IEEE Transaction on Electron Devices, Vol. ED-29(2), 306-315, February 1982.
5. C. T. Sah and A. Neugroschel, "Concentration profiles of recombination centers in semiconductor junctions evaluated from capacitance transients," IEEE Trans. Elec. Dev. Vol. ED-23(9), 1069-1074, September 1976.
6. Guo-Gang Qin and C. T. Sah, "Theory of concentration profiling technique for semiconductors with many deep levels," Solid-State Electronics, Vol. 25(10), 1045-1053, October 1982.

III. TRAPPING LEVELS FROM ION IMPLANTATION DAMAGE

For micron and submicron silicon CCD's and other silicon VLSI and VHSIC transistors and integrated circuits, ion implantation is a major indispensible technology used to produce properly doped thin surface layers on either a bare or oxidized silicon. Current projection of the next generation technology for 1 and 4 Megabit MOS dynamic memory indicates that a focused ion beam of submicron diameter will be an essential tool to produce the submicron features for these high density integrated circuits which require submicron device features. Such a foucsed ion beam technology would also be indispensible for large array silicon CCD devices.

An important but still unanswered question is the effect of ion implantation on the reliability or operating life of micron and submicron devices and on their resistance to radiation during operation. It is clear that the kinetic energy of a 10 to 100 keV ion beam used in the ion implantation technology is many orders of magnitude higher than the thermal energy, about 0.1 eV, available during the conventional annealing and activation processes at 900 to 1100C, used in the ion implantation technology. Since there is probably little local melting and recrystallization at these low temperatures of 900 to 1100C, an important question is how much of the radiation damage has been completely removed by annealing. Another important and unanswered question is if indeed most of the damage are 'annealed' so that they are electrically activated as shallow dopant levels or electrically inactivated as deep level traps, then is the crystal environment around these activated and inactivated traps the same as those in the original crystal which did not undergo an ion implantation process? This second question is important for radiation hardness and for long term reliability. If the environment is not completely restored to that of a non-implanted crystal, then one would expect the environment (i.e. locations of the silicon atoms surrounding the 'annealed' defect) to be 'soft' or much easier changed by subsequent ionizing radiation, hot electron impact whose kinetic energy is sufficient to break these weak bonds, or even thermal hole capture whose energy release (a few electron-volts) in the oxide would be sufficient to break these weak bonds. These effects would reduce the radiation hardness and operating life of devices and circuits employing ion implantation technology compared with those which do not; but there are probably no silicon devices and circuits which do not require the use of the ion implantation technology.

In the past and at the present, there has been little concern and critical study to resolve the above questions since it seemed that a about-900C-anneal or heat treatment will completely remove the ion implant damage (i.e. render them electrically inactive) and it will also completely activate the shallow-level dopant impurities, such as boron, phosphorus, arsenic or antimony. Due to this 'temporary fix', our knowledge of the atomic nature and chemical composition of the many deep and shallow levels arising from ion implantation damage is still very inadequate.

Another hindrance to a thorough and in-depth study of the traps produced by ion implantation is the complexity of the problem. There are many levels produced which were first reported by Sah and his students in 1971 and a detailed but very preliminary complilation of the levels was reported in 1976 [7,8]. These closely spaced levels complicate the analysis of the capacitance transient spectra very substantially. In addition, very substantial 'annealing' or deactivation of these defect levels occurs in the 25C to 500C range so that most of the levels would become inactivated and invisible in the capacitance transient spectra if precautions are not taken during diode fabrication, such as thermo-compression wire bonding and thermal die bonding, as well as annealing or/and contact sintering around 400C or 500C.

The very important advances made by Professors Li and Qin, described in section III, on the measurement techniques and theory have made it possible to do an in-depth study of the properties of the energy levels generated by ion implantation and their atomic and chemical makeups. Without these experimental and theoretical advances, the proposed goals would be impractical to attain.

The principle objectives in this study are: (i) to characterize the deep and shallow levels from ion implantation damage, including the measurements of the energy levels, the thermal capture and emission rates of electrons and holes at these levels; (2) to determine the density profiles of these levels as a function of annealing time in a wide range of annealing temperature; (3) to determine the annealing kinetics from the time dependence of the density profiles; and (4) to delineate the atomic and chemical models of the defect centers from these measurements as well as from the variation of the impurities (oxygen, carbon, transition and refractory metals) that are originally present in the crystal or introduced during the fabrication of the test diodes.

The first milestones of the project were reached when Professor Qin demonstrated the new techniques for multiple levels in ion implanted silicon diodes [9]. The principal conclusions are: (1) the theory developed is adequate and readily implemented in a computer controlled setup; (2) there are more than 8 levels whose DLTS peak temperatures lay within 77 to 220K; (3) the trap density profile is highly peaked; (4) the trap density profile lags or is shallower than the majority carrier or implanted boron concentation profile; (5) many of the peaks anneal out below about 500C; and (6) a complex annealing and 'reverse anneal' or generation occur around 420C. In addition, the CVCT is highly non-exponential as expected while the CCVT is and can generally be decomposed into several exponentials due to the closely spaced energy levels. A detailed account has been published [9].

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7. W. Chan and C. T. Sah, "Defect centers in boron-implanted silicon," Journal of Applied Physics, Vol.42(11), 4768-4773, November 1971.
8. C. T. Sah, "Bulk and interface imprefections in semiconductors," Solid-State Electronics, Vol.19(12), 975-990, December 1976.
9. Quo-gang Qin, Ming-Fu Li and C. T. Sah, "Deep level profiles in boron implanted n-Si," J. Appl. Phys. Vol.53(7), 4800-4811, July 1982.

At the writing of this final report, a very comprehensive study is in progress on the annealing behavior of the levels in the upper half of the energy gap in boron-implanted silicon diodes similar to those reported in Professor Qin's paper [9]. In addition, the low temperature dewar has been modified using a close-cycle helium refrigerator to reach a sample temperature of 10K. This lowered temperature enabled measurements of very shallow levels (about 50 mV from the band edge). Two very large DLTS peaks have been observed below 77K, one at 25K and the other at 62K. At present, it has not been established if the 25K peak is due to a level or due to the substrate resistance or RC time constant effect from the deionization of the shallow phosphorus level in the boron-implanted n-type silicon.

Systematic measurements of the annealing kinetics as a function of annealing time at each given annealing temperature are now in progress from about 250C to 600C. The upper range will be extended in subsequent measurements when specially designed epitaxial diodes are used to study the completeness of annealing at annealing temperature above 800C.

The support of Professors Li and Qin were entirely from their government. Professor Qin's three-month extension to complete his second paper [9] was supported by a private fund. No USAF nor any federal funds were used to support Professor Li and Qin.

The continuation work has been carried out by Daniel Briant Jackson, a graduate student in electrical engineering whose support has come from a IBM Predoctoral Fellowship in the last two years.

IV. NEW METHOD FOR MEASUREMENT OF BOTH MAJORITY AND MINORITY CARRIER CAPTURE RATES AT THERMAL EQUILIBRIUM IN ONE DIODE

One of the major problems encountered by previous workers using the capacitance transient methods to detect the presence of traps in the semiconductor energy gap is the inability to precisely determine the minority carrier capture rates at thermal equilibrium. This parameter is needed in the design of transistors and integrated circuits where lifetime and leakage are important limitations, such as CCD devices in which the lifetime would control the recovery rate and hence the speed with which the device can be clocked. There are many other operating parameters of transistors and integrated circuits which would also rely on these parameters.

In the past, minority carrier capture rates have been determined using a second diode with opposite bulk conductivity type but there is no assurance that the level seen in the second diode is the same as the level in the first diode. Thus, there is a very strong need to have a method to measure both the majority carrier and minority carrier capture rates in one diode.

The new method is based on the constant-voltage capacitance transient technique but the diode is forward biased with short pulses to strategically control the trapped majority as well as the minority carrier densities. The size of the capacitance transient decay after the cessation of the forward biased pulse then gives rise to the required information on the minority carrier capture rate. The deviation from the conventional zero-bias pulsed technique for the determination of the majority carrier capture rate is that the pulse extend to forward bias and the forward current magnitude is accurately determined and accurately related to the injected minority carrier density at the positions which will then be spanned by the depletion layer during the reverse bias when the thermal-emission capacitance decay is measured. The key quantity determined experimentally is the minority carrier density which enables one to determine the minority carrier capture at thermal equilibrium accurately.

In addition, the new method also allows us to determine very large majority and minority carrier capture rates, which would normally give recombination lifetimes of one nanosecond or less. This is too short to detect using conventional techniques employing the one mega Hertz capacitance meter due to circuit loading and RC time constant limitations of the C-meter.

The new technique has been tested on silicon diodes diffused with gold, zinc, sulfur and doped with titanium. A paper giving the theory as well as experimental demonstration of the technique is in preparation. No preprint will be available for inclusion in this final report. An article will appear in a 1984 issue of the Journal of Applied Physics.

V. LOW FIELD IMPACT IONIZATION RATE

Interband impact generation of electron-hole pairs in silicon CCD is thought to be one of the major and ultimate limitations on the performance of this device. The reason is that as the device dimension shrinks, the electric field in the CCD gaps would increase. Many electron-hole pairs can be generated by electrons crossing the high-field gaps. This generation is aided by repeated and multiple transits through the many gaps, so that its effect could be important even at relatively low fields.

To estimate this effect, the interband impact generation rate of electron-hole pairs must be known with reasonable accuracy. This is not the case at present. The purpose of this study was to determine this low field impact ionization rate using the CCD structure itself. After some tests, a 2-micron gate, one-layer metal, and circular race-track or carrousel-like structure was selected in 1976 during the predecessor contract. Many attempts were made to fabricate this structure by a graduate student. Preliminary diagnostic results were obtained and device design revisions were made [10]. No revised device structures were fabricated due to the early termination of the contract.

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10. J. Detry, Ph.D. thesis, to be published as a RADC technical report.

VI. TWO-DIMENSIONAL COMPUTER-AIDED-ANALYSIS

Multi-dimensional analysis is required to predict the performance of micron and submicron CCD and other silicon VLSI and VHSIC devices, since the device dimension transverse to current flow are shrunk to sizes comparable to the dimension longitudinal or parallel to the current flow. The effects of impact ionization as well as charge injection which would degrade the performance and life respectively are highly dependent on the electric field which are particularly high at the corners of these two- and even three-dimensional device structures. Thus, a two-dimensional numerical analysis effort was undertaken in this program. Here, another visiting professor from China was instrumental in providing the expertise during his two-year tenure at ISSEL.

A program was developed to determine the effect of channel width on the threshold voltage of an inversion channel, such as those in MOSFET's and in CCD's. The fringe field at the edge of the narrow gate electrode would penetrate into the channel region and increase the threshold voltage. In addition, due to the sharp corners, the fringe field would be very high, increasing the rate of interband impact ionization, avalanche hot electron or hole injection, as well as dielectric breakdown.

The results of this work are described in detail in three papers, two of which have been published [11,12] and a third to appear in December, 1983 [13]. Two other papers on the new boundary equations will probably be published in 1984 [14,15].

The first task was to produce a unique and quantitative definition of the threshold voltage so that it can be both measured unambiguously by a well defined set of experimental conditions and computed theoretically again by the same set of conditions. This was accomplished and reported [11,12]. The threshold voltage is defined from the drain conductance versus d.c. gate voltage curve at zero drain-to-source d.c. voltage. The threshold gate voltage is then the intercept of the tangent to the conductance-gate voltage curve at the gate-voltage axis or x-axis. This definition satisfies the theoretical and experimental criteria just outlined and in addition, it can be easily measured, even in a production environment.

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11. C. T. Sah, "The narrow gate effect in silicon VLSI MOSFET," Proc. of Technical Papers, 1983 Inter. Symp. on VLSI Technology, Systems and Applications, pp.165-169, Publisher: ERSO, ITRI, Hsinchu, Taiwan(311)
12. Chao-Ren Ji and C. T. Sah, "Two-dimensional numerical analysis of the narrow gate effect in MOSFET," IEEE Trans. Electron Devices, Vol. ED-30(6), 635-647, June 1983.
13. Chao-Ren Ji and C. T. Sah, "Analysis of the narrow gate effect in submicron MOSFET's," IEEE Trans. Electron Devices, Vol. ERD-30(12), 1100-1108, December 1983.
14. C. T. Sah and Chao-Ren Ji, "Physical finite-difference boundary condition at the insulator-semiconductor interface for two-dimensional numerical device analyses," to be published.
15. Chao-Ren Ji and C. T. Sah, "Improved finite differnce equations for solving Poisson's equation in non-uniformly doped semiconductor," to be published.

The second task was to select the numerical technique to solve the Shockley equations for arbitrary device geometry and impurity doping profiles. Three techniques are available: the finite difference method, the finite element method and the equivalent circuit method. Although the last one was developed by Sah and his students and extensively used in the one-dimensional analysis, it was more complicated to master and to program than the finite difference method which is probably the simplest among the three and which is certainly the one that has the best tutorial documentation in text books. Thus, it was decided to use this method since the visiting staff had no previous computer programming nor numerical analysis experiences and in addition, it provides us with some experience on this most popular technique so that we can make future comparisons with our equivalent circuit model.

During the development of the finite difference solution techniques, some new and accurate methods to implement the boundary conditions were discovered, developed and put through accuracy tests [14,15]. They provided significant improvements in accuracy and speed for finding the numerical solutions. At a quick glance (as claimed by the reviewers of our papers listed as references [12] to [14]), the new finite difference boundary equation seems to be derivable from more general formulations, one of which was given in a Vargas 1962 textbook. However, a closer inspection suggests that our development is more accurate and provides a procedure to deal with more general impurity variations than the other formulations. The finite difference equation was instrumental in enabling us to get accurate solutions (tested against known one-dimensioinal analytical solutions) using only 80 KB of memory of a Hewlett-Packard 1000F 16-bit minicomputer system, and in a reasonably short time.

The computer results of the threshold voltage of narrow gate MOS FET's were compared with experimental measurements and the agreement was good, especially since all the conditions of measurements were not given in the published experimental results. Plans were made to remeasure these narrow gate MOSFET's. The devices were obtained from a former graduate student in the aerospace industry where the narrow-gate MOSFET's were fabricated. Measurements have not started.

Sample numerical analyses were also made with considerable success for devices with tapered oxides and ion implanted field regions, using the finite difference program.

One of the main objectives was to develop accurate analytical and approximate formulae based on the device physics so that the formulae can be used to predict the narrow gate effects in a CAD package. In addition, the formulae should have a minimum number of parameters which can be either computed using the two-dimensional program or measured from a test transistor structure or test pattern. A two-parameter model is developed which is shown to be highly accurate [12] for micron wide gates. A more complicated procedure is required when the gate width shrinks below one micron and the fringe field penetrates into the midgap position [13].

VII. INTERFACE STATES AND TRAPS ON OXIDIZED SILICON

Oxide traps, interface states and silicon bulk traps are all very detrimental to the performance of silicon VLSI and VHSIC transistors and integrated circuits, as well as their reliability. These same traps have similar deleterious effects on the reliable operation and performance of silicon CCD devices. One of the particular areas of concern in CCD signal processing devices is the effect of trapping of the charge packets at the interface states of the oxide/silicon interface.

Extensive efforts have been undertaken by Sah and his graduate students on the delineation and characterization of these surface traps on oxidized silicon. These are all supported by other contracts and grants. But some of the work on interface states are partially supported by this AF contract in view of their possible relevance to charge transfer efficiency in CCD devices.

The main findings are summarized. All of the interface states seem to be attributable to dangling oxygen and dangling silicon bonds at the oxide/silicon interface. Their concentration is affected by the oxide growth and subsequent high temperature device fabrication conditions as well as the crystallographic orientation of the silicon surface prior to the oxide growth.

These dangling bonds can trap electrons or holes and serve as electron-hole recombination and generation sites.

These dangling bonds may be rendered electrically inactive, i.e. no longer capable of trapping an electron or a hole, if they are saturated or tied up by hydrogen. We have obtained extensive experimental evidence which shows that atomic hydrogen (not molecular hydrogen, ionized hydrogen atom or proton) is the impurity which can neutralize these dangling bonds and inactivate the interface traps electrically. Furthermore, the bonded hydrogen can be released by energetic electron impact if the energetic electron has more than about 4 eV of kinetic energy, since the hydrogen bond energy with all of the elements is about this value. The bonded hydrogen can also be released by the capture of a thermal hole in the oxide since the silicon dioxide energy gap is about 9 eV so that a hole capture would impart as much as 4 eV or more energy to the hydrogen bond, thereby releasing the atomic hydrogen from the bond site [16,17].

The hydrogen deactivation phenomenon is even observed in the surface space charge layer of silicon [17]. Here, the boron, gallium, aluminum and indium acceptors are all found to be deactivated if atomic hydrogen is present or transported to this silicon surface region from the aluminum gate.

The most important practical result is that hydrogen and hydrogen containing species are completely gettered from the MOS system when a silicon gate is heated to above 900C, a procedure commonly used in silicon gate technology but its water and hydrogen gettering property is probably not recognized as the origin of highly stable devices.

---

16. C. T. Sah, Jack Sun and Joe Tzou, J. Appl. Phys. 54(2),944-956(1983).
17. C. T. Sah, Jack Sun and Joe Tzou, App.Phys.Lett. 43(2),204-206(1983).

VIII. PUBLICATIONS

This section provides a list of publications supported by this contract in part or in whole.

8.1 Y. C. Sun and C. T. Sah
Interface and edge effect and its contribution to the frequency dispersion of MOS admittance
Solid-State Electronics, v24, 569-576, 1981

8.2 M. F. Li and C. T. Sah
New techniques of capacitance-voltage measurements of semiconductor junctions
Solid-State Electronics, v25, 95-99, 1982

8.3 M. F. Li and C. T. Sah
A new method for the determination of dopant and trap concentration profiles in semiconductors
IEEE Trans. Electron Devices, ED-29(2), 306-315, Feb. 1982

8.4 G. G. Qin, M. F. Li and C. T. Sah
Deep level profiles in boron implanted n-Si
Journal of Applied Physics, v53(7), 4800-4811, July 1981.

8.5 G. G. Qin and C. T. Sah
Theory of concentration profiling technqiue for semiconductors with many deep levels
Solid State Electronics, v25(10), 1045-1053, October 1982.

8.6 C. T. Sah
The narrow gate effect in silicon VLSI MOSFET
Proc. Tech. Papers, Inter. Symp. on VLSI Technology, 165-169, March, 1983.

8.7 C. R. Ji and C. T. Sah
Two-dimensional numerical analysis of narrow gate effect in MOSFET
IEEE Trans. Electron Devices, ED-30(6), 635-647, June 1983.

8.8 C. R. Ji and C. T. Sah
Analysis of the narrow gate effect in submicron MOSFET's
IEEE Trans. Electron Devices, ED-30(12), 1100-1108, December 1983.

8.9 Alex C. Wang and C. T. Sah
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XI. STAFF

9.1	C. T. Sah	Professor and Principal Investigator
9.2	James Detry	Ph.D.E.E., now with Gould, Inc.
9.3	Jack Sun	Ph.D.E.E., now with IBM Research
9.4	Dan Jackson	Ph.D.E.E., pending
9.5	Joe Tzou	Ph.D.E.E., now with AMD, Sunnyvale,CA
9.6	Phil Chan	Assistant Prof., now with INTEL, Santa Clara
9.7	Alex Wang	Ph.D. Physcis pending
9.8	*L. M. Fu	Visiting Professor, returned to China.
9.9	*G. G. Qin	Visiting Professor, returned to China.
9.10	*C. R. Ji	Visiting Professor, returned to China.
9.11	Dale Hitt	Senior E.E., continuing
9.12	Toshi Nishida	Senior Physics, continuing
9.13	Kit Stanton	Junior, secretarial, departed
9.14	Nancy Yacko	B.S.C.S., now with Hewlett-Packard
9.15	Dave Schaffer	Junior EE, continuing
9.16	Cathy Wren	Graduate student, secretarial assistant
9.17	Mary Rasmusson	B.S.C.S., now at Burrough, San Diego
9.18	Tom Liu	B.S.E.E., now with Bell Labs.
9.19	Louis Guido	M.S.E.E., now with Bell Labs.
9.20	Mike Wojtowicz	M.S.E.E., pending, at TRW Los Angeles.
9.21	Bob Richie	M.S.E.E., pending

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* These three members are not U.S. citizen nor U.S. permanent residence. All other members are.

Legend: B.S.E.E. = Bachelor of Science degree in Electrical Engineering
B.S.C.S. = Bachelor of Science degree in Computer Science

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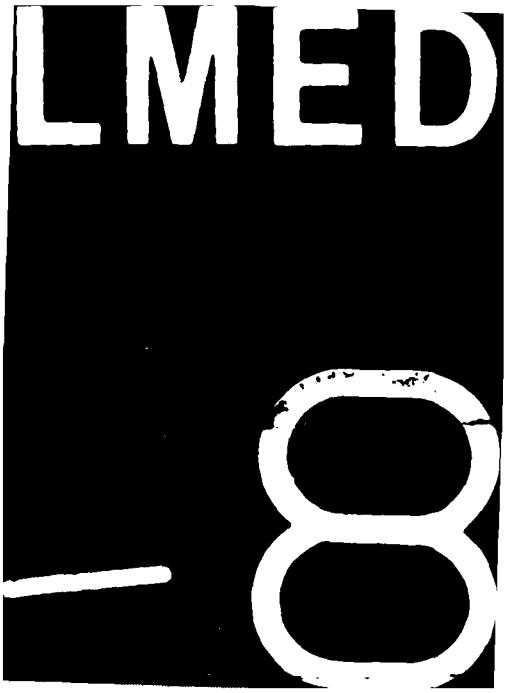
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